Amendments to the Specification

Please amend the paragraph beginning at page 8, line 2, as follows;

In the preferred embodiment, the nodes 1-6 of the subject invention are utilized to compile data by capturing a signal having an instantaneous value. The signal is considered to have the value as sampled at whatever moment in time the sampling occurs, i.e., an instantaneous value. In addition, the signal contains no other information other than the instantaneous value. The preferred embodiment compiles a plurality of instantaneous measured values (data) during a testing of a vehicle. In particular, during servo-hydraulic testing of a vehicle on a testing platform. Of course, the subject invention is in no way limited to this envisioned application. The distributed multiprocessing system 30 of the subject invention can be used in virtually any industry to perform virtually any type of computer calculation or processing of data.

Please amend the paragraph beginning at page 9, line 3, as follows;

The first processor 40 processes information at a first station, i.e., node 1's location, and assigns a first address to a first processed information. Specifically, the first processor 40 captures the signal having the instantaneous value and assigns the first address to the captured instantaneous value to define a first instantaneous value. Similarly, a second processor 42 processes information at a second station, i.e., node 2's location, and assigns a second address to a second processed information. Specifically, the second processor 42 captures the signal having the instantaneous value and assigns the second address to the captured instantaneous value to define a second instantaneous value. As should be appreciated, the addresses are indexed to correlate to the indexing of the processors 40, 42 and the nodes 1-6.

Please amend the paragraph beginning at page 9, line 14, as follows. It is noted that previous amendments to this paragraph have been incorporated.

As shown in Figures 5 and 7, the first 40 and second 42 processors further include a hardware portion 48 for assigning the first and second addresses to the first and second processed information (first and second instantaneous values), respectively. In particular,

the hardware portion 48 assigns a destination address onto the processed information corresponding to the identifier of an addressed node 1, 2 . The hardware portion 48 also conforms or rearranges the data or information to an appropriate format. As discussed above, the processors 40, 42 can be of different types which recognize different computer formats. Hence, the hardware portion 48 ensures that the proper format is sent to the addressed node 1, 2 . However, the addresses are preferably of a common format such that the hub 32 commonly recognizes these signals. Examples of the processors 40, 42 operation are discussed below in greater detail.

Please amend the paragraph beginning at page 11, line 16, as follows. It is noted that previous amendments to this paragraph have been incorporated.

As also shown in Figures 5 and 7, each task 62 includes at least a pair of pointers 64, 66 for directing a flow of data or values from a sending node 1, 2 to a destination node 1, 2 . The pointers 64, 66 are illustrated as branching off of the fourth task 62 in Figure 5 and the third task 62 in Figure 7. As should be appreciated, there are pointers 64, 66 associated with each of the tasks 62 such that there is a continuous stream of information. The pointers 64, 66 includes a next task pointer 64 for directing the sending node 1, 2 to a subsequent task 62 to be performed, and at least one data destination pointer 66 for directing the sending node 1, 2 to forward the processed information (instantaneous values) to the hub 32. Preferably, there is only one next task pointer 64 such that there is a clear order of operation for the processors 40, 42. Conversely, there may be any number of data destination pointers 66 such that the sending node 1, 2 may simultaneously forward processed information to a multitude of addressed nodes 1-6. Further, each of the processed information sent to the multitude of addressed nodes 1-6 may be different.

Please amend the paragraph beginning at page 12, line 12, as follows;

As shown back in Figures 1, 2, and 3, a first communication link 68 interconnects the first processor 40 of node 1 and the hub 32 for transmitting the first processed information, such as the first instantaneous value, between the first processor 40 and the hub 32. Similarly, a second communication link 70 interconnects the second processor 42

of node 2 and the hub 32 for transmitting the second processed information, such as the second instantaneous value, between the second processor 42 and the hub 32. As appreciated, the hub 32 is capable of receiving processed information (instantaneous values) from all of the nodes 1-6 simultaneously and then forwarding the processed information to the correct destinations.

Please amend the paragraph beginning at page 13, line 12, as follows. It is noted that previous amendments to this paragraph have been incorporated.

As shown in Figure 3, the central routing hub 32 includes a sorter 72 for receiving at least one of the first and second processed information (first and second instantaneous value) from at least one of the first 40 and second 42 processors. By receiving the processed information, at least one sending node 1-6 is defined. Each of the first 40 and second 42 processors of the nodes 1, 2 may send processed information or only one of the first 40 and second 42 processors of the nodes 1, 2 may send processed information. In any event, at least one of the nodes 1-6 will be deemed as a sending node 1-6 .

Please amend the paragraph beginning at page 13, line 19, as follows. It is noted that previous amendments to this paragraph have been incorporated.

The hub 32 and sorter 72 also identify a destination of at least one of the first and second addresses of the first and second processed information (first and second instantaneous value), respectively to define the destination address. Finally, the hub 32 and sorter 72 send at least one of the first and second processed information without modification from the hub over at least one of the communication links 68, 70 to at least one of the nodes 1, 2. The node 1, 2 to which the information is being sent defines at least one addressed node 1, 2. The sorter 72 includes hardware 74 for determining the destination addresses of the addressed nodes 1-6.

Please amend the paragraph beginning at page 14, line 15, as follows;

As will be discussed in greater detail below, the send-only system 30 eliminates the duplication of stored data or values. Preferably, the first 76 and second 80 incoming

transmission lines and the first 78 and second 82 outgoing transmission lines are unidirectional optical fiber links. The optical fiber links are particularly advantageous in that the information is passed under high speeds and becomes substantially generic. Further, the unidirectional optical fiber links prevent the possibility of data collision. As appreciated, the first 76 and second 80 incoming and the first 78 and second 82 outgoing transmission lines may be of any suitable design without deviating from the scope of the subject invention.

Please amend the paragraph beginning at page 14, line 23, as follows. It is noted that previous amendments to this paragraph have been incorporated.

The distributed multiprocessing system 30 can include any number of additional features for assisting in the uninterrupted flow of data (values) through the system 30. For example, a counter may be included to determine, control, and limit a number of times processed information is sent from a sending node to an addressed node 1-6. A sequencer may also be included to monitor and control a testing operation as performed by the system 30. In particular, the sequencer may be used to start the testing, perform the test, react appropriately to limits and events, establish that the test is complete, and switch off the test.

Please amend the paragraph beginning at page 17, line 21, as follows;

Referring to Figure 16, node 1 is shown again in greater detail. The method comprises the steps of processing information within at least one of the first 40 and second 42 processors for capturing a signal having an instantaneous value. In this example the information is processed within the first processor 40 by proceeding through a number of tasks 62 in node 1. As discussed above, the tasks 62 may be any suitable type of calculation, compilation or the like. Preferably, the processing of the information is further defined as ~~creating data within the first processor 40. The creating of the data is further defined as~~ compiling a plurality of instantaneous measured values (data) ~~the data~~ within the first processor 40. During the testing of the vehicle, which is discussed only as an illustrative embodiment, many of the processors of the nodes 1-6, including in this example node 1, will obtain and compile testing data in the form of instantaneous measured values.

Please amend the paragraph beginning at page 18, line 24, as follows. It is noted that previous amendments to this paragraph have been incorporated.

The processed information (values) from the fourth task 62 is then addressed and transmitted from the first processor 40 across at least one of the communication links 68, 70 toward the hub 32. As discussed above, the communication links 68, 70 are preferably unidirectional. Hence, the step of transmitting the processed information is further defined as transmitting the processed information across the first incoming transmission line 76 in only one direction from the first processor 40 to the hub 32 to define a send-only system 30. The transmitting of the processed information is also further defined by transmitting the data (instantaneous values) along with executable code from the sending node 1-6 to the addressed node 1-6. As appreciated, the first 40 and second 42 processors initially do not have any processing capabilities. Hence, the executable code for the processors 40, 42 is preferably sent to the processors 40, 42 over the same system 30. Typically, the executable code will include a command to instruct the processors 40, 42 to process the forwarded data (values) in a certain fashion. It should also be noted that the transmitting of the processed information may be a command to rearrange or reorganize the pointers of the processor of the addressed node 1-6. This in turn may change the order of the tasks which changes the processing of this processor. As appreciated, the transmitted processed data may include any combination of all or other like features.

Please amend the paragraph beginning at page 20, line 23, as follows. It is noted that previous amendments to this paragraph have been incorporated.

As shown in Figure 19, the processed information (instantaneous value) is then stored within the second real memory location 56 of the addressed node 2 wherein the second processor 42 can utilize the information (value) as needed. The processed information may be stored within the categorized message areas or locations of the second real memory location 56 in accordance with the associated memory address. The destination address (of node 2) may be stripped from sent processed information before the information is stored in the second real memory location 56.

Please amend the paragraph beginning at page 21, line 6, as follows;

As also discussed above, the method of operation for the subject invention eliminates unnecessary duplication of information. When node 1 sends the processed information to the hub 32, which then travels to node 2, the information, which can include data, such as the instantaneous value, executable code, or both, is not saved at node 1 and is only stored at node 2. Node 2 does not send a confirmation and node 1 does not request a confirmation. Node 1 assumes that the information arrived at node 2. The subject system 30 is used to transport data (values) to desired real memory locations where the data (value) can be used during subsequent processing or evaluation.